TRANSLATION OF KOREAN PRIORITY APPLICATION NO. 10-2003-0047491

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METHOD OF FABRICATING SEMICONDUCTOR DEVICE HAVING SUBMICRON LINEWIDTH

SUMMARY

[Abstract]

The present invention relates to a method of fabricating a semiconductor device using a hard mask and, more particularly, a method of removing a hard mask as an etching mask in fabricating a semiconductor device having a submicron linewidth by using a hard mask and an existing light source.

An object of the present invention is achieved by a method of fabricating a semiconductor device having a submicron linewidth, comprising a first step of depositing oxide on a substrate, a second step of depositing polysilicon on the oxide, a third step of forming a hard mask on the polisilicon, a fourth step of depositing and patterning photoresist on the hard mask, a fifth step of etching the polysilicon by using a pattern formed through the hard mask, and a sixth step of etching the hard mask.

Accordingly, by using a hard mask instead of a photoresist mask and existing equipment without additional investments and controlling a required linewidth by products through an etching process, a semiconductor device fabrication method according to the present invention embodies a product having a submicron linewidth. Thus, the present invention can realize expandability of process, extension of generality, and maximization of productivity in the production line.

The present invention removes selectively a hard mask on a gate electrode through a wet etching using gaseous HF while gate oxide under the gate electrode is protected. Thus, the present invention obviates a problem that a residual hard mask obstructs formation of silicide when silicide is formed by using a refractory metal after formation of spacers, thereby improving a device operation speed.

[Representative Drawing]

Fig. 4

[Index Word]

Hard mask, KrF, ArF, gate electrode, wet etching, HF, vapor phase cleaning

SPECIFICATION

[Title of the invention]

Method of Fabricating Semiconductor Device having Submicron Linewidth

[Brief description of the drawings]

Fig. 1 is a cross-sectional view illustrating a process of depositing and patterning oxide, polysilicon, a hard mask, and photoresist on a semiconductor substrate.

Fig. 2 is a cross-sectional view illustrating a process of removing photoresist.

Fig. 3 is a cross-sectional view illustrating a process of etching polysilicon using a pattern formed through a hard mask.

Fig. 4 is a cross-sectional view illustrating a process of removing a hard mask.

Fig. 5 is a cross-sectional view illustrating a process of forming spacers on sidewalls of a gate.

[Detailed description of the invention]

[Object of the invention]

[Technical field of the invention and background of the related art]

The present invention relates to a method of fabricating a semiconductor device using a hard mask and, more particularly, a method of removing a hard mask as an etching mask in fabricating a semiconductor device having a submicron linewidth by using a hard mask and an existing light source.

Photolithography is a micro processing technology which has supported a progress of semiconductor device industry. Resolution enhancement in the photolithography is in charge of the future of high-integration semiconductor device.

Lithography is generally a patterning process and divided into a photo process and an engraving process. In recent years, however, lithography has come to mean only the photo process, and is classified into optical and non-optical lithography based on a used light source. In a semiconductor device process, the lithography is a technology to form a circuit on a substrate, comprising processes of coating photoresist on a substrate, transmitting light through a mask so that the photoresist reacts with the light, developing the photoresist to form a pattern, and embodying a desired pattern by engraving the substrate with the photoresist pattern.

The degree of integration of a semiconductor chip has increased by a factor of about 4 times every 3 years. In the photolithography process, there have been many developments in materials such as CAR (chemically amplified resist), in processing aspects such as TLR (tri-layer resist), BLR (bi-layer resist), TSI (top-surface imaging), ARC (anti-reflective coating), etc., and in mask aspects such as a PSM (phase shift mask), OPC (optical proximity correction) etc., as well as in exposure equipment itself such as a lens having high numerical aperture and hardware.

Early generation exposure equipment included a contact printer that employed an exposing method, where a mask was located on an upper portion of a substrate to be close to the substrate, and an operator manually adjusted the focus of the optical system with the naked eye. Then, as the technology developed, the resolution was enhanced by reducing the gap between the mask and the substrate, and exposure was achieved through soft contact or hard contact (lower than 10 μm), according to the gap size.

In the early 1970s, a projection-type exposure equipment, which employed an optical system using reflection or refraction, was developed. Accordingly, advancements such as improvement of resolution and an increase in the life of a mask as well as wafer size scale-up, were actively applied to product developments. After that, in the mid-1970s, a stepper applying projection optics was developed to substantially contribute to mass production of semiconductors.

The stepper, adopting an exposure method of "step and repetition," made a turning point in the development of photolithography. By using exposure equipment adopting the stepper method, accuracy in setting as well as resolution was enhanced. The early stepper adopted a reducing projection exposure method using a mask to be patterned on a substrate by a reduction ratio of about 5:1 or about 10:1. However, the ratio of about 5:1 became gradually in common use due to limitations in mask pattern and size.

In early 1990s, a scanner adopting an exposure method of "step and scanning" was developed. The scanner type exposure equipment was able to cope with increasing chip size and raise productivity, although it put a heavy burden on a mask pattern by using a reduction ratio of 4:1. The resolution of photolithography is closely related to a wavelength of a light source. Early exposure equipment using g-line (λ=436nm) was able to form a pattern of about 0.5 μm, and exposure equipment using i-line (λ=365nm) was able to form a pattern of about 0.3 μm.

Recently, exposure equipment using a KrF laser (λ=248nm) as a light source, new photoresist materials and development of incidental technologies have made it possible to form a pattern having a design rule lower than 150 nm.

Now, developing technology is capable of forming a fine pattern less than 110 nm by using exposure equipment employing an ArF laser (λ=193nm). DUV (Deep ultra-violet) photolithography has high resolution and a good DOF (depth of focus) property compared to the i-line, but it is difficult to control processes. Such a process control problem may be optically caused by a short wavelength and chemically by using a chemically amplified photoresist. As the wavelength becomes shorter, a CD (critical dimension) tilting phenomenon due to a static wave effect and an engraving phenomenon of reflective light due to a substrate phase become more severe.

In fabricating a semiconductor device having a submicron linewidth, which cannot be formed by existing equipment, a method to solve limitations of a photolithography process is to

adjust bias, i.e., difference between a value of critical dimension of the photoresist pattern before etching (DI CD) and a value of critical dimension after etching (FI CD). However, although this method is used, it is not easy to cope with a margin of linewidth that is being reduced.

One embodiment is presented to describe the present invention in detail although the present invention can be embodied by various methods.

For example, when a gate having 90 nm linewidth is formed by using existing KrF equipment, a marginal linewidth patterned by a photolithography process is about 125 nm and, therefore, the difference 35 nm has to be removed by an etching process. In view of a DUV photoresist height (PR height), this is an impossible process. Accordingly, a special method, for example, using an ArF scanner, is required. That is, in the KrF process, a height of photoresist has to be less than 3000Å considering a DOF (depth of focus) margin although 125 nm linewidth is patterned.

As a result, to achieve a gate CD (channel length) of 90 nm, the difference 35 nm has to be removed by an etching process. Therefore, each side of a gate pattern has to be cut by 17.5 nm by using photoresist, but in this case a uniform gate device cannot be formed because of an etching speed ratio of gate material to photoresist.

To solve such a problem, a hard mask layer is formed on an etch-target layer and a PR pattern is formed on the hard mask. The PR pattern is formed more thinly than a conventional PR pattern. Next, an etching process is performed using the PR pattern to form a hard mask pattern having the same size as the PR pattern.

Then, the etch-target layer is etched using the hard mask pattern as a mask to form an etch-target layer pattern having a desired size.

Next, the hard mask is removed by a dry etching process. However, conventional art cannot completely remove the hard mask on the substrate because of difference in process uniformity between a dry etching process and a film deposition process. Thus, a residual hard mask obstructs reaction between polysilicon and refractory metal such as titanium or cobalt in a later silicide formation process to lower contact resistance, thereby increasing contact resistance. The increase of contact resistance may cause deterioration of device reliability.

[Technical problem]

Accordingly, the present invention is directed to a method of fabricating a semiconductor device having a submicron linewidth that substantially obviates one or more problems due to limitations and disadvantages of the related art. The present invention provides a method of removing a hard mask using gaseous HF in embodying a submicron linewidth, which cannot be formed by using an existing light source, by applying a hard mask process to logic products.

[Disclosure of the invention]

The object of the present invention is achieved by a method of fabricating a semiconductor device having a submicron linewidth, comprising a first step of depositing oxide on a substrate, a second step of depositing polysilicon on the oxide, a third step of forming a hard mask on the polysilicon, a fourth step of depositing and patterning photoresist on the hard mask, a fifth step of etching the polysilicon using a pattern formed through the hard mask, and a sixth step of etching the hard mask.

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Figs. 1 through 5 illustrate a semiconductor device fabrication process in accordance with the present invention.

Fig. 1 is a cross-sectional view illustrating a process of patterning photoresist using a mask.

First, oxide (11), polysilicon (12), a hard mask (13) and photoresist (14) are deposited on a semiconductor substrate (10). The photoresist (14) is patterned by using a mask to form a structure of Fig. 1. In detail, a thermal oxide layer as gate oxide is grown on a substrate on which an active area is defined, and polysilicon is then grown on the thermal oxide layer. A hard mask for patterning a gate is deposited on the top of the polysilicon and a photolithography process is performed using photoresist. The photoresist (14) is patterned by a KrF light source so that the width of a pattern formed is 120 nm. The hard mask (13) is preferably formed of SiH_4 oxide by PE-CVD. A thickness of the hard mask is preferably between about 150 Å and about 400 Å.

An anti-reflection coating (ARC) to reduce reflexibility may be further deposited on the hard mask. The anti-reflection coating is formed of organic or inorganic ARC.

Fig. 2 is a cross-sectional view illustrating a process of etching the hard mask and removing the photoresist.

The hard mask (13) is etched by using plasma and the photoresist pattern (14) as an etching mask. The plasma etching uses SF_6 gas and isotropically etches the hard mask. After the plasma etching, ashing/strip processes are performed to remove the photoresist.

Fig. 3 is a cross-sectional view illustrating a process of etching the polysilicon using a plasma etching to form a gate electrode.

To form a gate electrode, the polysilicon (12) is etched by a plasma etching using a hard mask pattern obtained after the ashing/strip processes as an etching mask. By the above-mentioned processes, a gate linewidth of a desired CD (critical dimension) can be formed. The plasma etching uses Cl_2/HBr, Cl_2/O_2, or HBr/O_2 as an etching gas so that an etching speed ratio of polysilicon : oxide is about 10:1. The width of a gate electrode formed by the above-

described process is 80 nm, which is less than 120 nm achieved by using a KrF light source. A residual product polymer, which is produced during polysilicon etching, is removed by using dilute HF cleaning.

Fig. 4 is a cross-sectional view illustrating a process of removing the hard mask by using HF.

The hard mask on the polysilicon is selectively removed by 39% HF solution gasified while the polysilicon and gate oxide are protected by the hard mask.

39% HF solution is gasified and the substrate is located on a hot plate to etch the substrate including the gate electrode. Here, the thermal oxide layer as gate oxide is etched at an etching rate less than 1 Å/min, the PE-CVD SiH_4 oxide of the hard mask is etched at an etching rate more than 200 Å/min, and the polysilicon is etched at an etching rate less than 1 Å/min.

A temperature of the hat plate is preferably between about 50℃ and about 90℃. The HF gas is generated from the surface of HF solution when N_2 gas with a temperature of more than 200℃ is sprayed on the surface of a chemical bath containing 39% HF solution.

Fig. 5 is a cross-section view illustrating a process of forming nitride spacers.

After removal of the hard mask, nitride spacers are formed and silicide is formed by using refractory metal to complete a gate device. An oxide layer (15) and nitride layer (17) are in sequence deposited on the substrate from which the hard mask is removed. The nitride layer is etched through an etch back process to form spacers (17).

In manufacturing a gate electrode, the above-described process can form a gate electrode having a linewidth of 90 nm by using an existing KrF light source and a hard mask instead of a photoresist mask.

In addition, by selectively wet etching the hard mask using 39% HF solution gasified, the present invention removes selectively the hard mask while protecting the gate oxide, thereby obviating a problem that a remaining hard mask residue prevents formation of silicide when silicide is formed using refractory metal after the formation of spacers.

The foregoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.

[Effect of the invention]

Accordingly, by using a hard mask instead of a photoresist mask and existing equipment without additional investments and controlling a required linewidth by products through an etching process in forming a gate electrode, a method of fabricating a semiconductor

device in accordance with the present invention embodies a product having a submicron linewidth. Thus, the present invention can realize expandability of process, extension of generality, and maximization of productivity in the production line.

The present invention removes selectively a hard mask on a gate electrode through a wet etching using gaseous HF while gate oxide under the gate electrode is protected. Thus, the present invention obviates a problem that a residual hard mask obstructs formation of silicide when silicide is formed by using a refractory metal after formation of spacers, thereby improving a device operation speed.

CLAIMS

【Claim 1】

A method of fabricating a semiconductor device having a submicron linewidth comprising:

a first step of depositing oxide on a substrate ;

a second step of depositing polysilicon on the oxide;

a third step of forming a hard mask on the polysilicon;

a fourth step of depositing photoresist on the hard mask and patterning the photoresist;

a fifth step of etching the polisilicon using a pattern formed through the hard mask; and

a sixth step of removing the hard mask;

【Claim 2】

The method as defined by claim 1, further comprising a step of depositing an anti-reflection coating on the hard mask to reduce reflexibility.

【Claim 3】

The method as defined by claim 2, wherein the anti-reflection coating is formed of organic or inorganic ARC.

【Claim 4】

The method as defined by claim 1, wherein patterning the photoresist in the fourth step is performed by using a KrF light source.

【Claim 5】

The method as defined by claim 1, wherein the hard mask is formed of SiH_4 oxide which is deposited by PE-CVD.

【Claim 6】

The method as defined by claim 1, wherein the hard mask has a thickness between about 150 Å and about 400 Å.

【Claim 7】

The method as defined by claim 1, wherein the pattern formed through the hard mask is formed by patterning the hard mask using a patterned photoresist as an etching mask and etching the hard mask.

【Claim 8】

The method as defined by claim 1, wherein etching the hard mask in the fifth step is an isotropic etching.

【Claim 9】

The method as defined by claim 1, wherein removing the hard mask in the sixth step is an wet etching which removes the hard mask while protecting the polysilicon and gate oxide by using 39% HF solution gasified.

【Claim 10】

The method as defined by claim 9, wherein the 39% HF solution gasified is formed through spraying N_2 gas with a temperature of more than 200 ℃ over the surface of a chemical bath containing HF solution so that gas is generated from the surface of the HF solution.

【Claim 11】

The method as defined by claim 9, wherein the wet etching is performed on a hot plate having a temperature between about 50 ℃ and about 90 ℃.

【Claim 12】

The method as defined by claim 9, wherein the wet etching is performed at an etching rate of less than 1 Å/min for the oxide and an etching rate of more than 200 Å/min for the hard mask.

DRAWINGS

Fig. 1

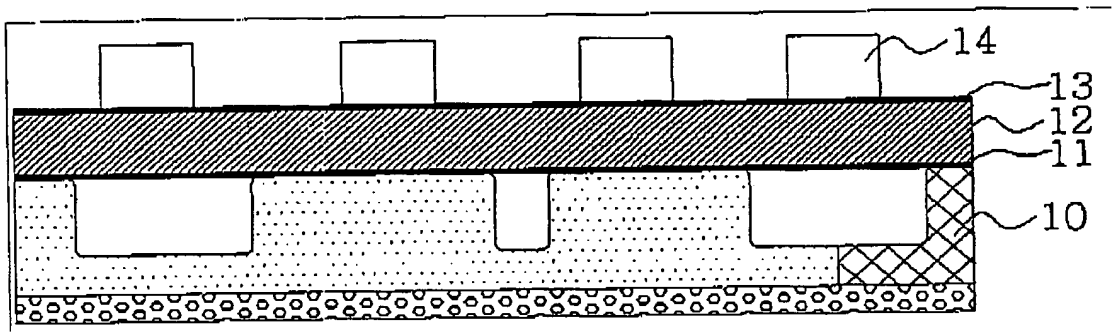


Fig. 2

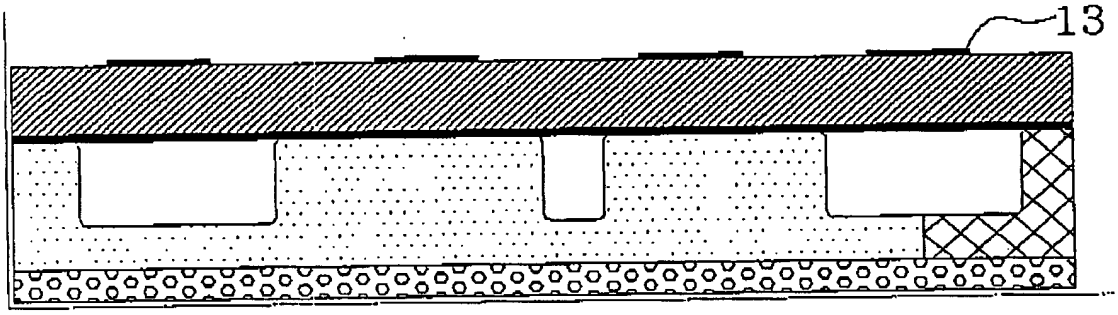


Fig. 3

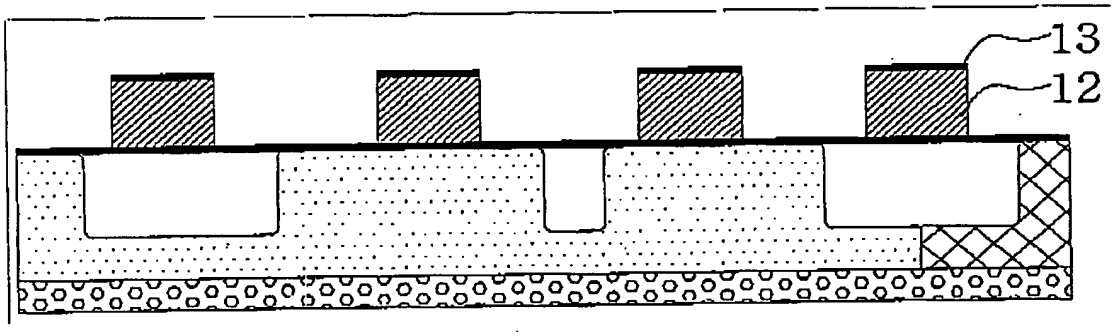


Fig. 4

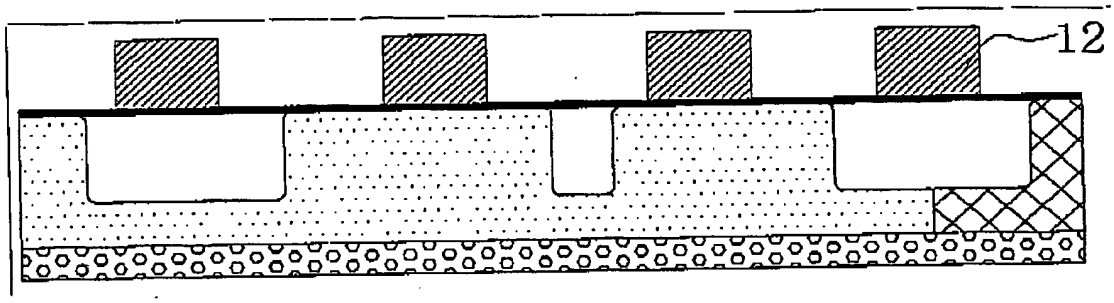
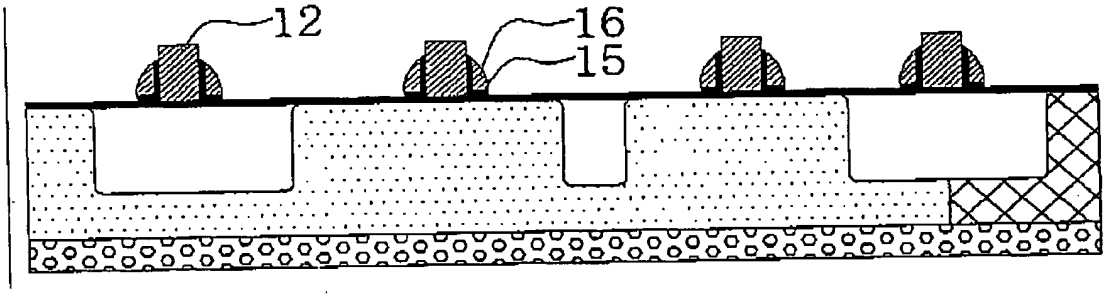


Fig. 5



I, So-Young OH, hereby certify that I am familiar with the Korean and English languages, and that the attached is a true and accurate translation of Korean Application 10-2003-0047491.

Date: September 15, 2005 Signature

Name So-Young OH